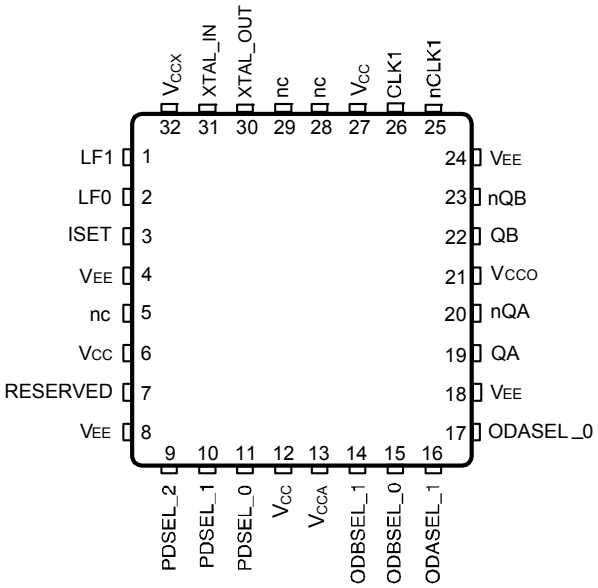
General Description

The IDT8V89308I is a PLL based synchronous multiplier specifically designed for applications utilizing Broadcom PHYs and Switches. This high performance device is optimized for Ethernet / SONET / PDH frequency translation and clock jitter attenuation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a low bandwidth PLL that is optimized to provide reference clock jitter attenuation. The second stage is a FemtoClock® frequency multiplier that provides the low jitter, high frequency Ethernet output clock that easily meets Gigabit and 10 Gigabit Ethernet jitter requirements. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in Ethernet, SONET, PDH applications. IDT8V89308I requires the use of an external, inexpensive fundamental mode crystal and uses external passive loop filter components which allows configuration of the PLL loop bandwidth and damping characteristics. The device is packaged in a space-saving 32-VFQFN package and supports industrial temperature range.

Features

- Two LVPECL output pairs
  Each output supports independent frequency selection at 25MHz, 125MHz and 156.25MHz
- One differential input supports the following input types: LVPECL, LVDS
- Accepts input frequencies 8kHz, 25MHz,125MHz and 155.52MHz
- First stage PLL bandwidth can be optimized for jitter attenuation and reference tracking using external loop filter connection
- FemtoClock frequency multiplier provides low jitter, high frequency output
- Absolute pull range: 50ppm
- FemtoClock VCO frequency: 625MHz
- RMS phase jitter @ 25MHz, using a 25MHz crystal (12kHz – 5MHz): 0.238ps (typical), 0.30ps (maximum)
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz – 20MHz): 0.223ps (typical), 0.30ps (maximum)
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (12kHz – 20MHz): 0.223ps (typical), 0.30ps (maximum)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Pin Assignment



IDT8V89308I
32 Lead VFQFN
5mm x 5mm x 0.925mm package body
NL Package
Top View

Block Diagram

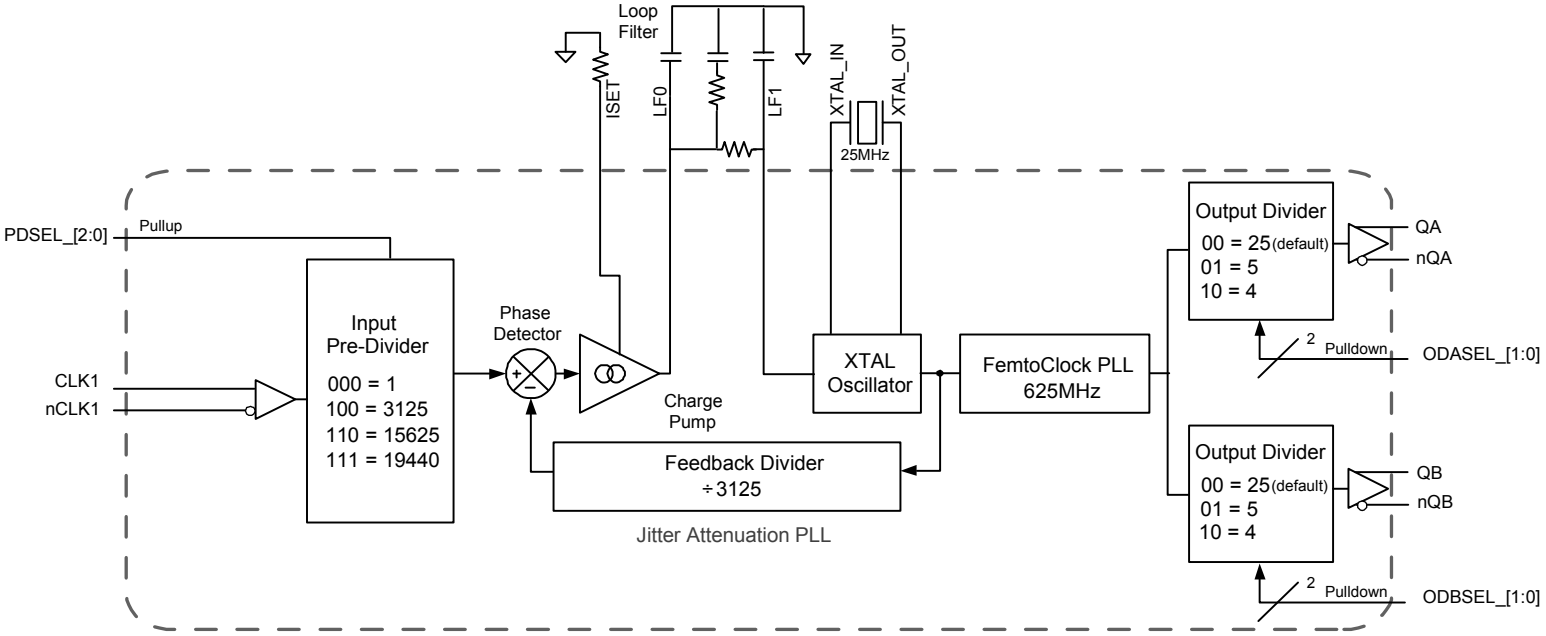


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/Output		Loop filter connection node pins. LF0 is the output. LF1 is the input.
3	ISET	Analog Input/Output		Charge pump current setting pin.
4, 8, 18, 24	V_{EE}	Power		Negative supply pins.
6, 12, 27	V_{CC}	Power		Core supply pins.
7	RESERVED	Reserved		Reserved pin. Do not connect.
9, 10, 11	PDSEL_2, PDSEL_1, PDSEL_0	Input	Pullup	Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A.
13	V_{CCA}	Power		Analog supply pin.
14, 15	ODBSEL_1, ODBSEL_0	Input	Pulldown	Frequency select pins for Bank B output. See Table 3B. LVCMOS/LVTTL interface levels.
16, 17	ODASEL_1, ODASEL_0	Input	Pulldown	Frequency select pins for Bank A output. See Table 3B. LVCMOS/LVTTL interface levels.
19, 20	QA, nQA	Output		Differential Bank A clock outputs. LVPECL interface levels.
21	V_{CCO}	Power		Output supply pin.
22, 23	QB, nQB	Output		Differential Bank B clock outputs. LVPECL interface levels.
25	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{CC}/2$ bias voltage when left floating.
26	CLK1	Input	Pulldown	Non-inverting differential clock input.
30, 31	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
32	V_{CCX}	Power		Power supply pin for charge pump.
5, 28, 29	nc	Unused		No connect.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Pre-Divider Selection Function Table

Inputs			
PDSEL_2	PDSEL_1	PDSEL_0	Pre-Divider Value
0	0	0	1
1	0	0	3125
1	1	0	15625
1	1	1	19440 (default)

Table 3B. Output Divider Function Table

Inputs		
ODxSEL_1	ODxSEL_0	Output Divider Value
0	0	25 (default)
0	1	5
1	0	4

Table 3C. Frequency Function Table

Input Frequency (MHz)	Pre-Divider Value	Crystal Frequency (MHz)	FemtoClock Feedback Divider Value	FemtoClock VCO Frequency (MHz)	Output Divider Value	Output Frequency (MHz)
0.008	1	25	25	625	25	25
0.008	1	25	25	625	5	125
0.008	1	25	25	625	4	156.25
25	3125	25	25	625	25	25
25	3125	25	25	625	5	125
25	3125	25	25	625	4	156.25
125	15625	25	25	625	25	25
125	15625	25	25	625	5	125
125	15625	25	25	625	4	156.25
155.52	19440	25	25	625	25	25
155.52	19440	25	25	625	5	125
155.52	19440	25	25	625	4	156.25

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.63V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{CC} -0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	33.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.20	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
V_{CCX}	Charge Pump Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				200	mA
I_{CCA}	Analog Supply Current				20	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	ODASEL_[1:0], ODBSEL_[1:0]	$V_{CC} = V_{IN} = 3.465V$			150	µA
		PDSEL_[2:0]	$V_{CC} = V_{IN} = 3.465V$			10	µA
I_{IL}	Input Low Current	ODASEL_[1:0], ODBSEL_[1:0]	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-10			µA
		PDSEL_[2:0]	$V_{CC} = 3.465$, $V_{IN} = 0V$	-150			µA

Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK1, nCLK1	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-10			µA
		nCLK1	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			V_{EE}		V_{CC} – 0.85	V

Common mode voltage is defined as the crossing point.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} – 1.10		V_{CCO} – 0.75	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} – 2.0		V_{CCO} – 1.6	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V. See Parameter Measurement Information section, *3.3V Output Load Test Circuit.*

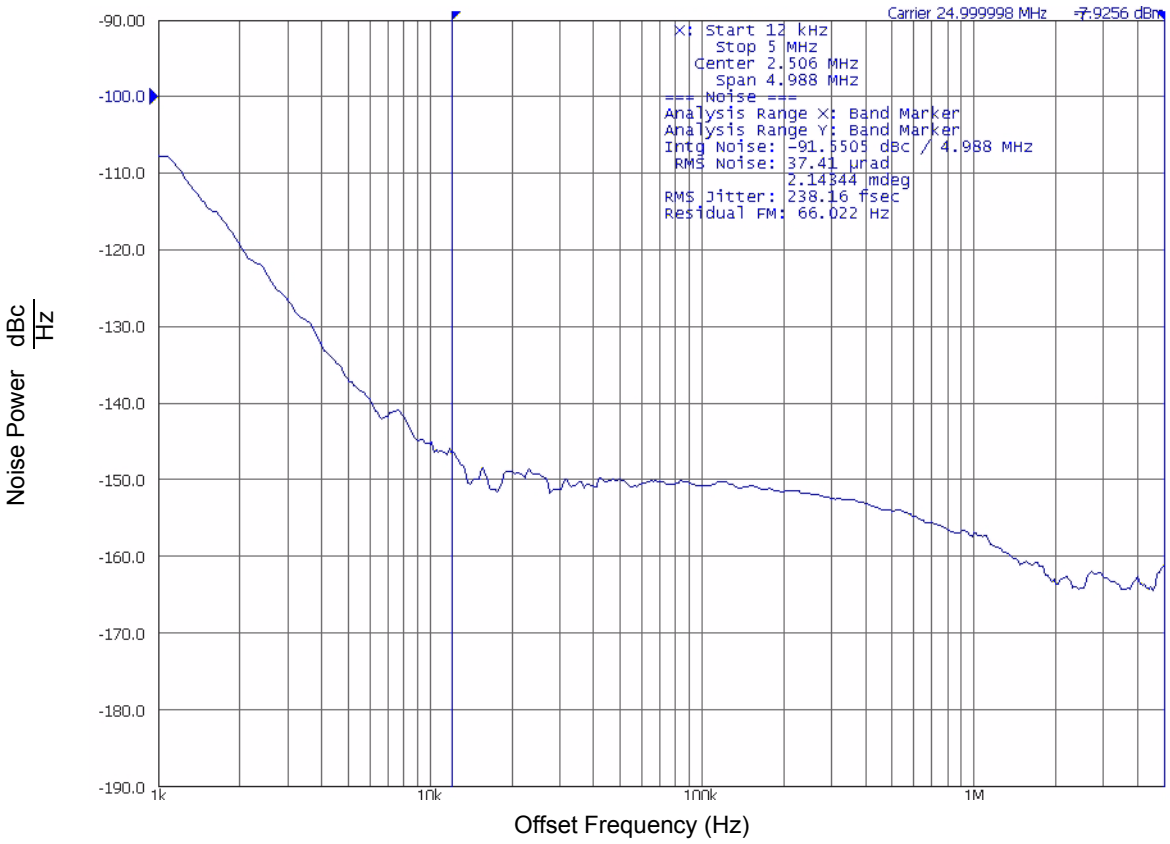
AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

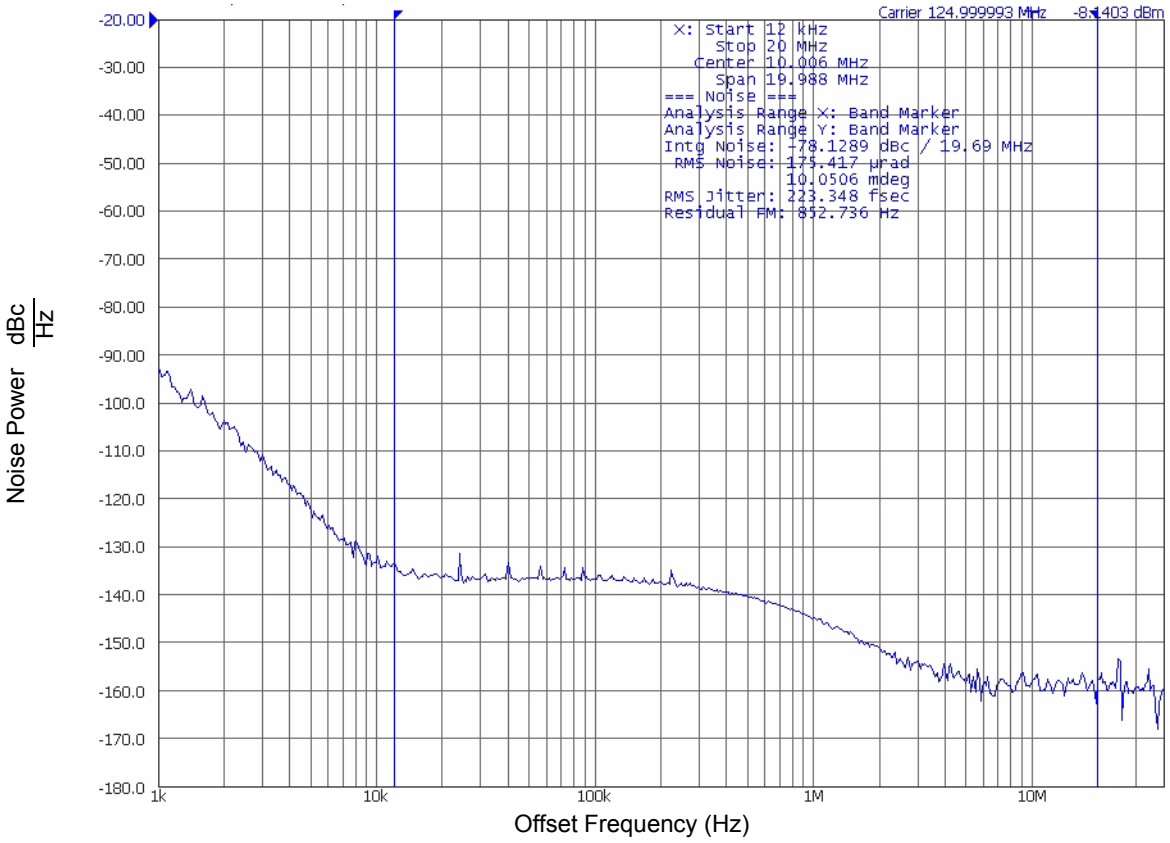
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency		0.008		155.52	MHz
f_{OUT}	Output Frequency		25		156.25	MHz
*t*jit(Ø)	RMS Phase Jitter, (Random), NOTE 1	f_{OUT} = 25MHz, 25MHz crystal, Integration Range: 12kHz – 5MHz		0.238	0.3	ps
*t*jit(Ø)	RMS Phase Jitter, (Random), NOTE 1	f_{OUT} = 125MHz, 25MHz crystal, Integration Range: 12kHz – 20MHz		0.223	0.3	ps
*t*jit(Ø)	RMS Phase Jitter, (Random), NOTE 1	f_{OUT} = 156.25MHz, 25MHz crystal, Integration Range: 12kHz – 20MHz		0.223	0.3	ps
*t*jit(pk-pk)	Peak-to-Peak Jitter	1e-12 BER			25	ps
*t*sk(o)	Output Skew; NOTE 2, 3				25	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	140		400	ps
odc	Output Duty Cycle		48		52	%
t_{LOCK}	XO & FemtoClock PLL Lock Time; NOTE 4			6		S

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using input frequency of 8kHz, QA/nQA and QB/nQB at the same frequency using 3rd order loop filter of 10Hz bandwidth. Refer to application schematics.
NOTE 1: Refer to the Phase Noise Plot.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 4: Lock Time measured from power-up to stable output frequency.

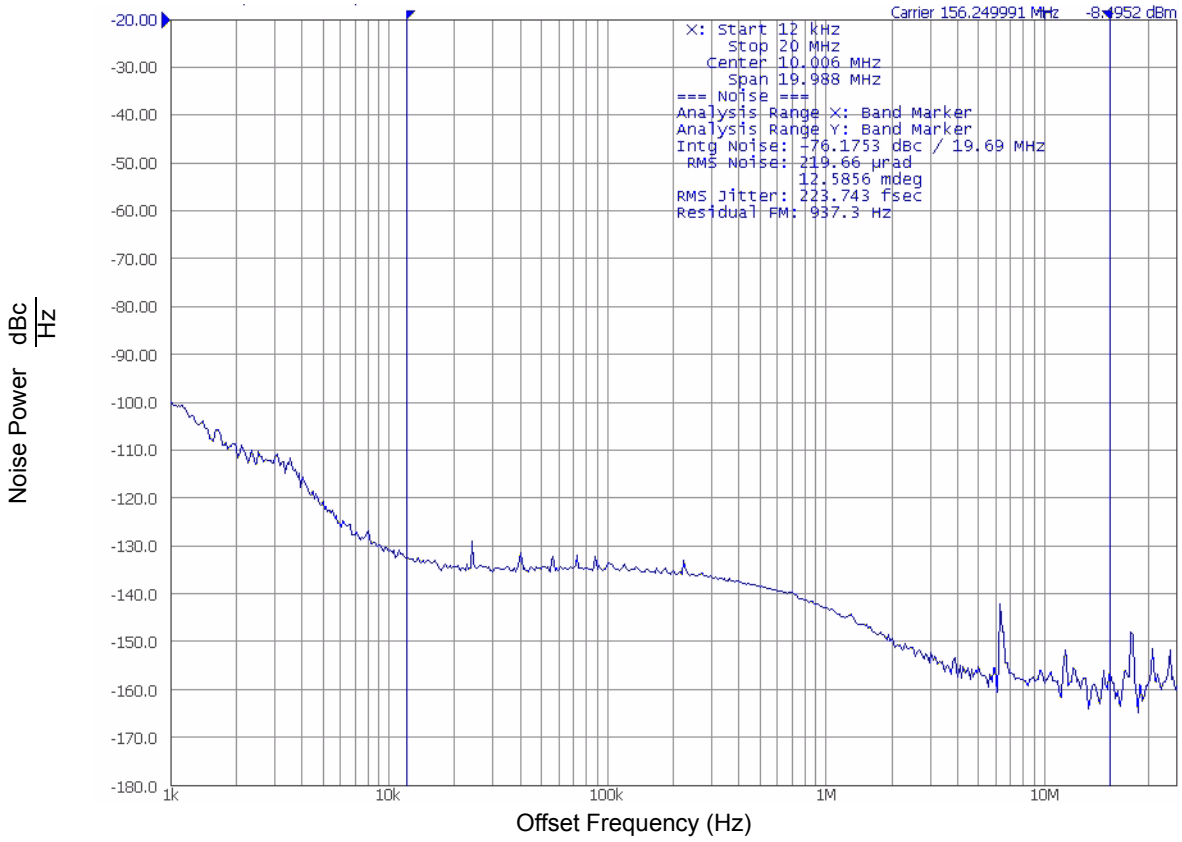
Typical Phase Noise *(25MHz)*



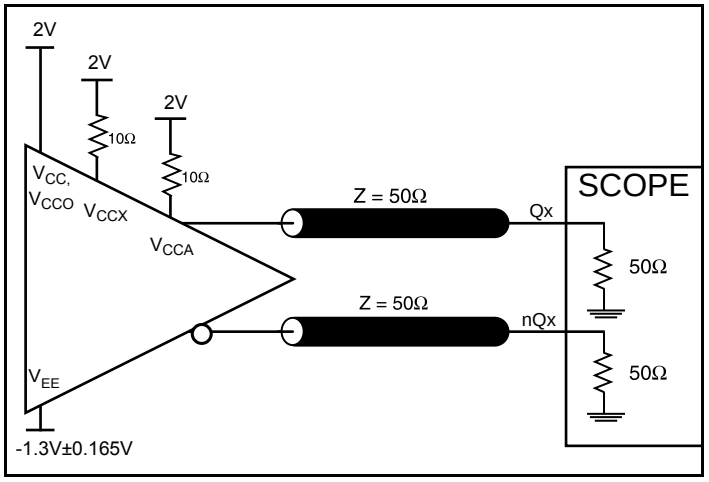
Typical Phase Noise *(125MHz)*



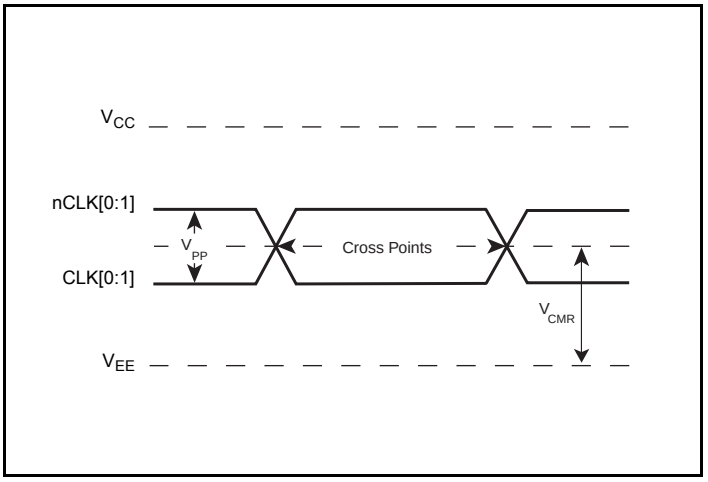
Typical Phase Noise *(156.25MHz)*



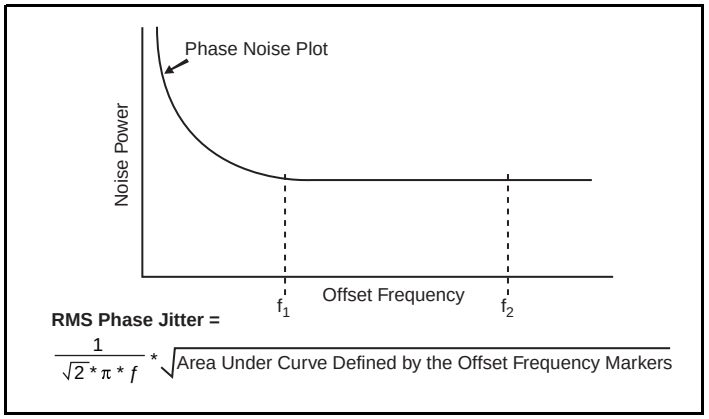
Parameter Measurement Information



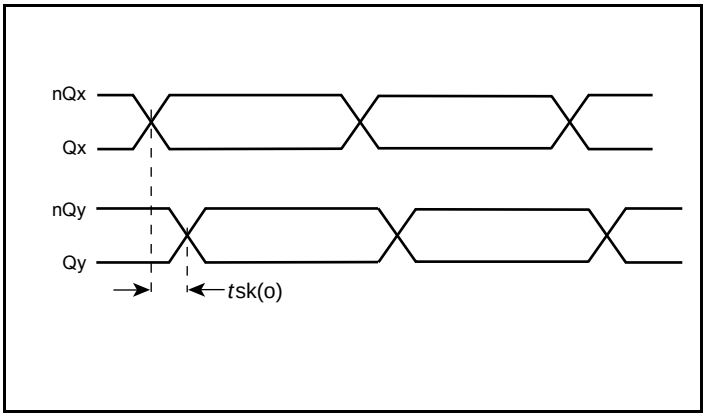
3.3V LVPECL Output Load AC Test Circuit



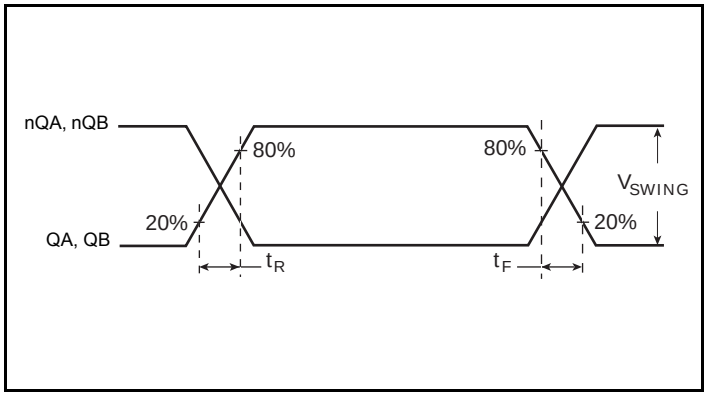
Differential Input Level



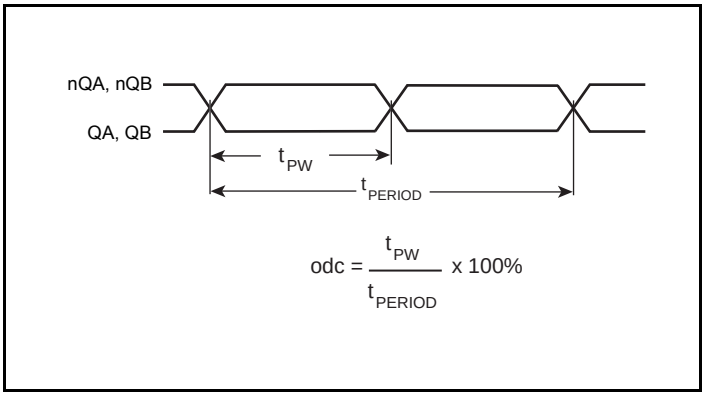
RMS Phase Jitter



Output Skew

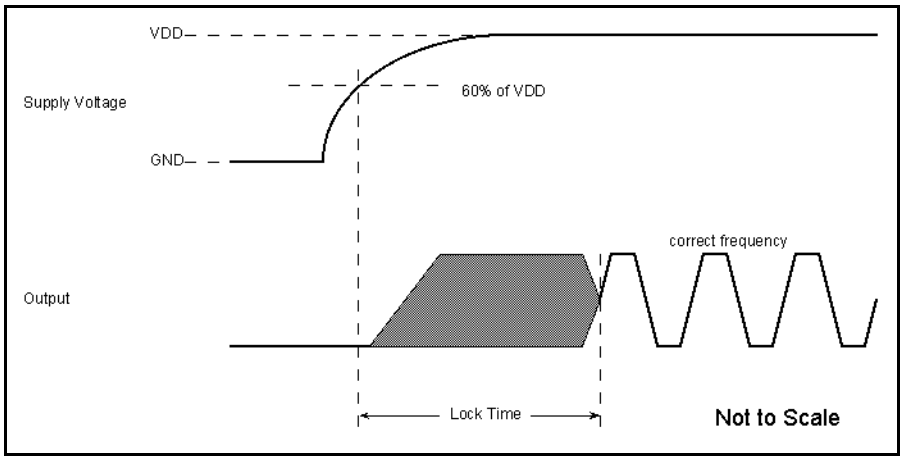


Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Parameter Measurement Information, continued



XO & FemtoClock PLL Lock Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

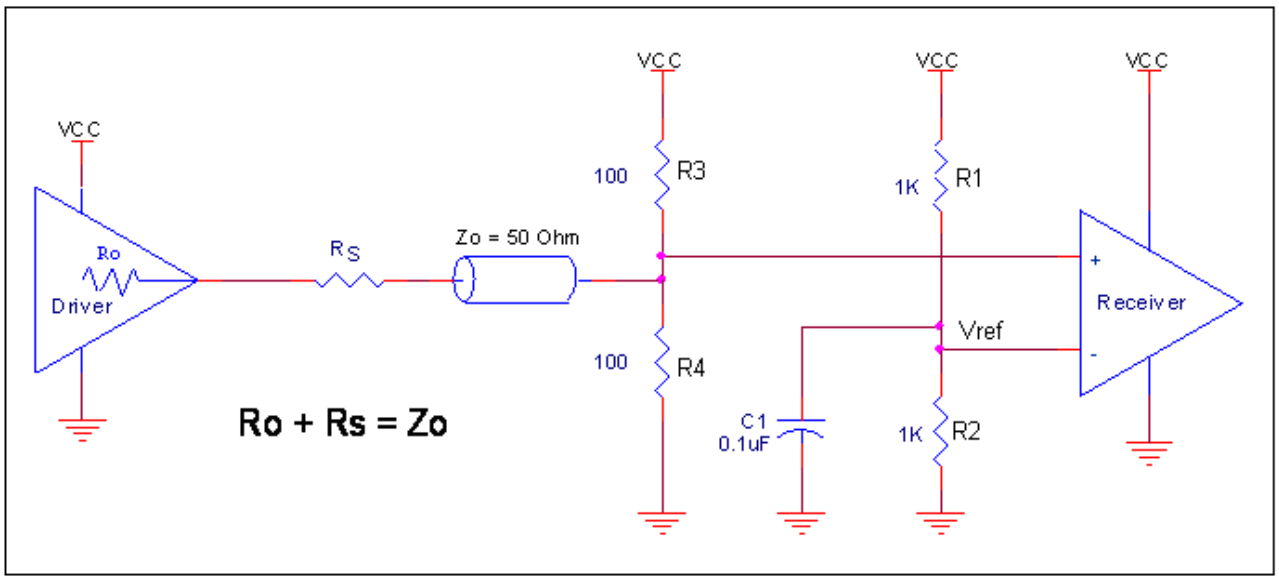


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2C* show interface examples for the CLK /nCLK input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

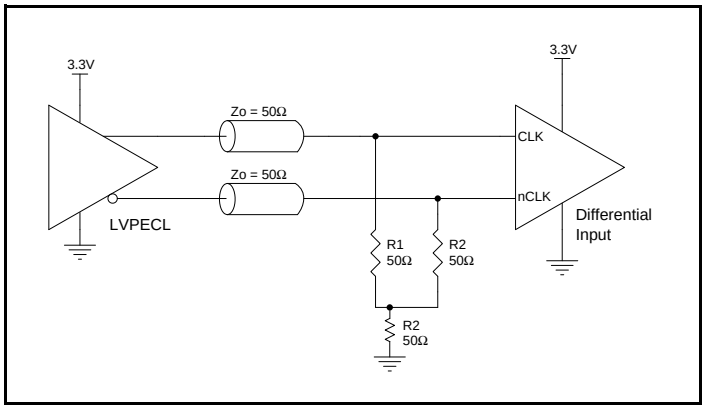


Figure 2A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

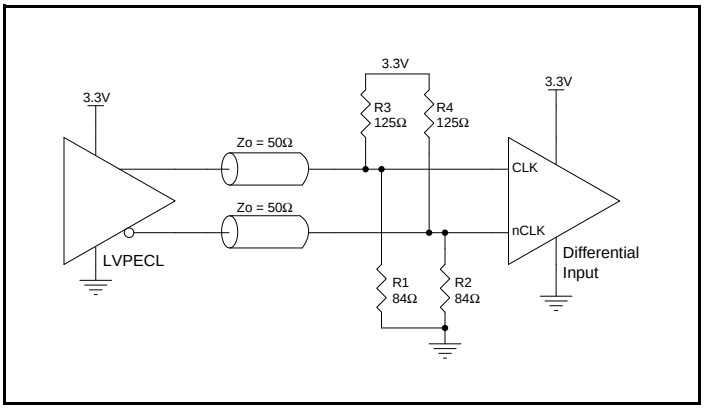


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

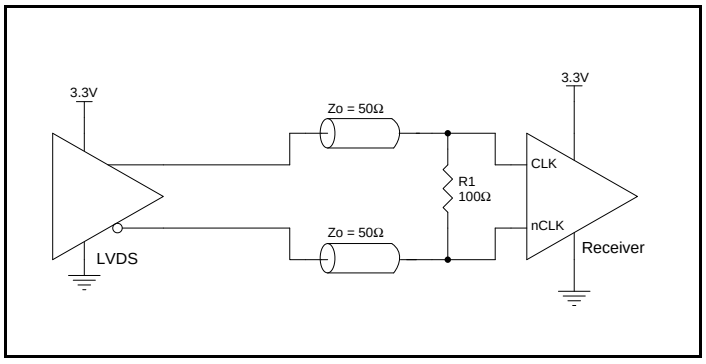


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVDS Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

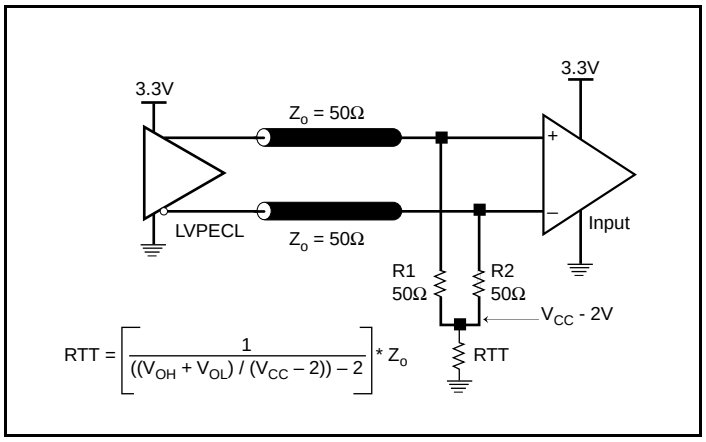


Figure 3A. 3.3V LVPECL Output Termination

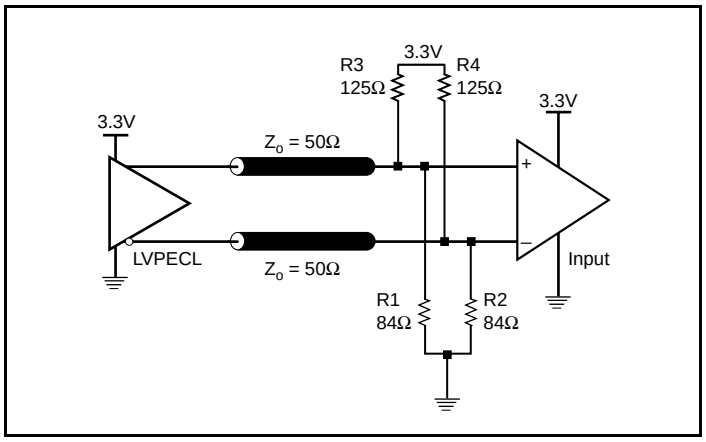


Figure 3B. 3.3V LVPECL Output Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

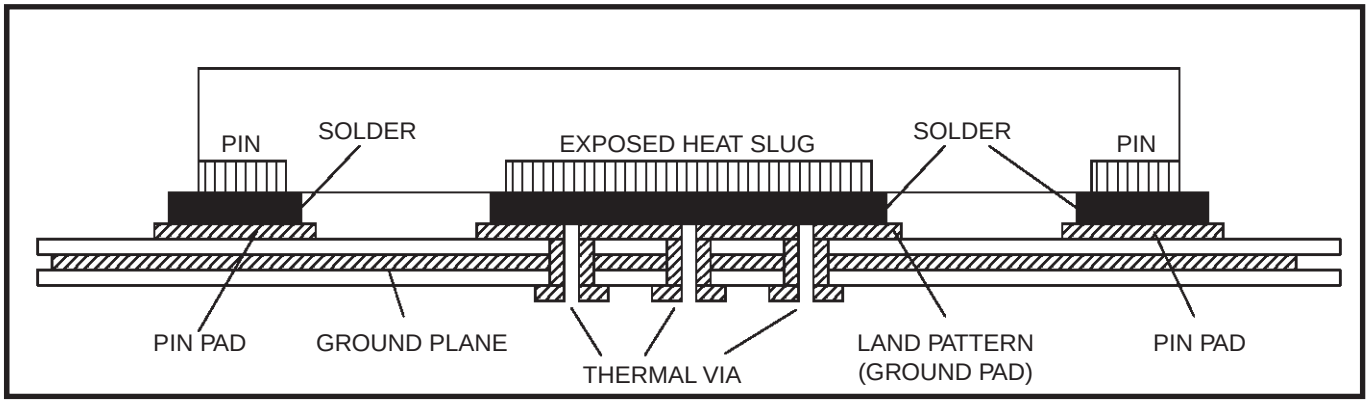


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Table 6. Crystal Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
	Mode of Oscillation			Fundamental		
f_N	Frequency			25		MHz
f_T	Frequency Tolerance			±20	±30	ppm
f_S	Frequency Stability			±20	±30	ppm
	Operating Temperature Range		-40		85	^{0}C
C_L	Load Capacitance			10	12	pF
C_O	Shunt Capacitance			4		pF
C_O / C_1	Pullability Ratio			220	240	
F_{L_3OVT}	3rd Overtone F_L		200			ppm
$F_{L\_3OVT\_spurs}$	3rd Overtone F_L Spurs		200			ppm
ESR	Equivalent Series Resistance				50	Ω
	Drive Level				1	mW
	Aging @ 25 ^{0}C				±3 per year	ppm

Application Schematic Example

Figure 5 (next page) shows an example of IDT8V89308I application schematic. In this example, the device is operated at V_{CC} = V_{CCX} = V_{CCA} = V_{CCO} = 3.3V. A 3-pole filter is used for additional spur reduction. As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8V89308I provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

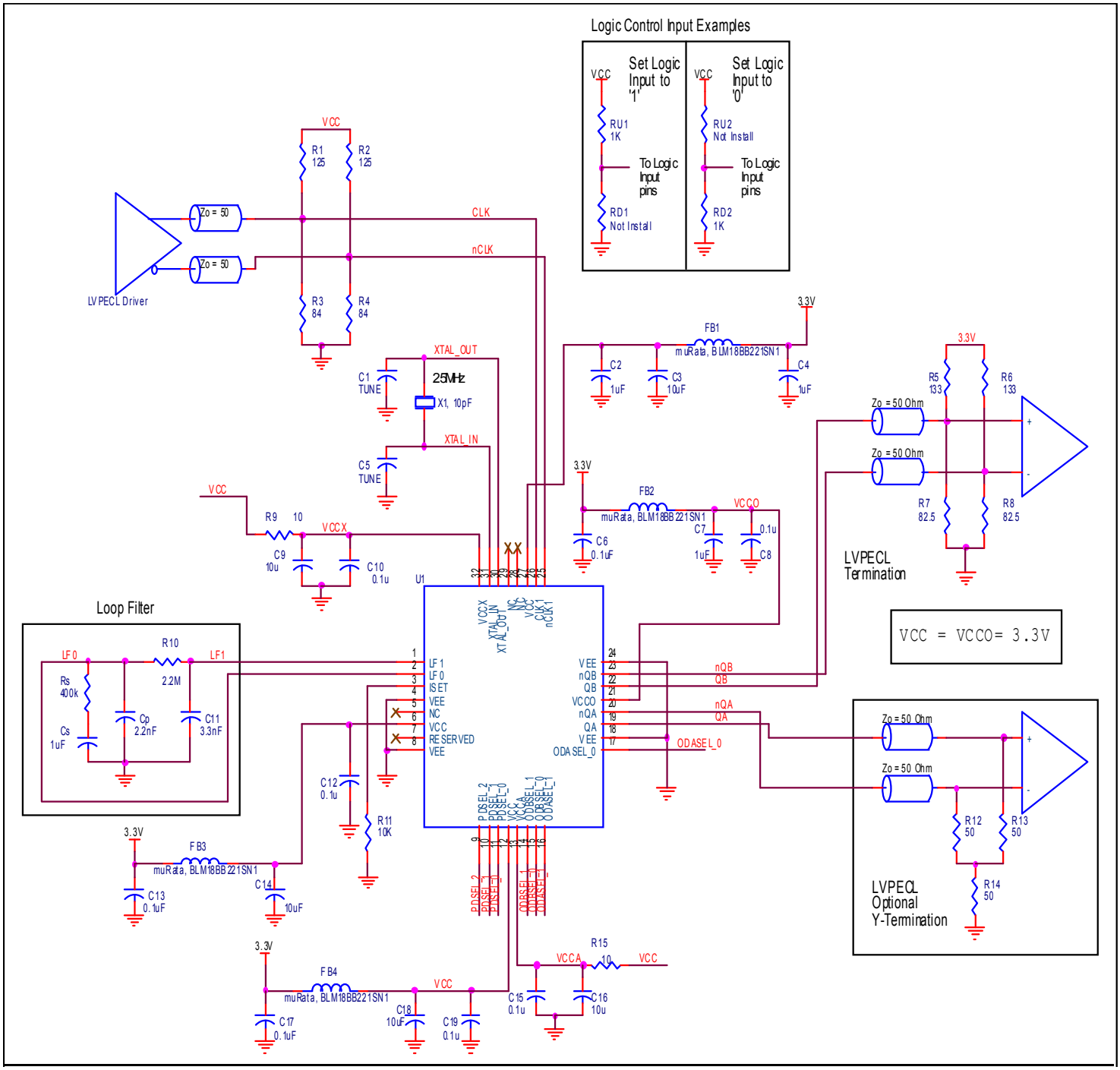


Figure 5. IDT8V89308I Application Schematic

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8V89308I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8V89308I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 200mA = **693mW**
- Power (outputs)$_{MAX}$ = **31.55mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 31.55mW = **63.1mW**

Total Power_$_{MAX}$ (3.465V, with all outputs switching) = 693mW + 63.1mW = **756.1mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and it directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.756W * 33.1°C/W = 110°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 6.*

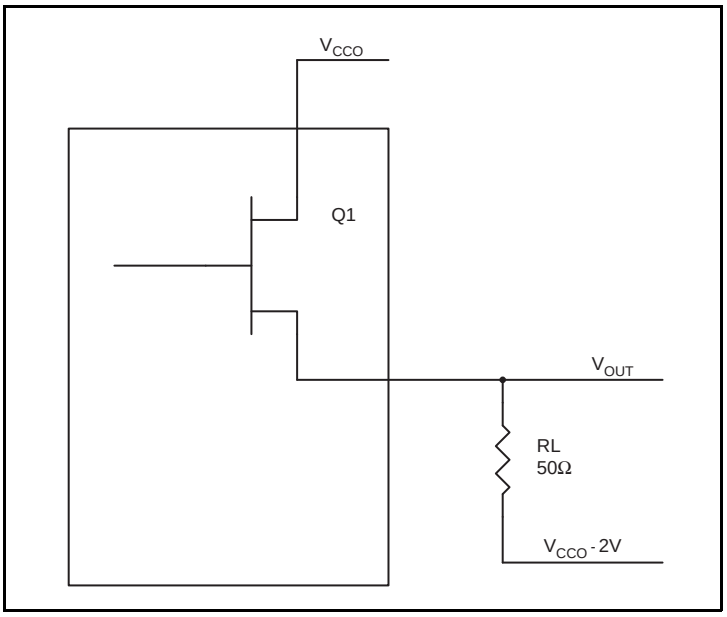


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **V_{CCO_MAX} – 0.75V**
  ($V_{CCO\_MAX} – V_{OH\_MAX}$) = **0.75V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **V_{CCO_MAX}** – **1.6V**
  ($V_{CCO\_MAX} – V_{OL\_MAX}$) = **1.6V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

Pd_H = [($V_{OH\_MAX} – (V_{CCO\_MAX} – 2V)$)/$R_L$] * ($V_{CCO\_MAX} – V_{OH\_MAX}$) = [(2V – ($V_{CCO\_MAX} – V_{OH\_MAX}$))/$R_L$] * ($V_{CCO\_MAX} – V_{OH\_MAX}$) = [(2V – 0.75V)/50Ω] * 0.75V = **18.75mW**

Pd_L = [($V_{OL\_MAX} – (V_{CCO\_MAX} – 2V)$)/$R_L$] * ($V_{CCO\_MAX} – V_{OL\_MAX}$) = [(2V – ($V_{CCO\_MAX} – V_{OL\_MAX}$))/$R_L$] * ($V_{CCO\_MAX} – V_{OL\_MAX}$) = [(2V – 1.6V)/50Ω] * 1.6V = **12.80mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.55mW**

Reliability Information

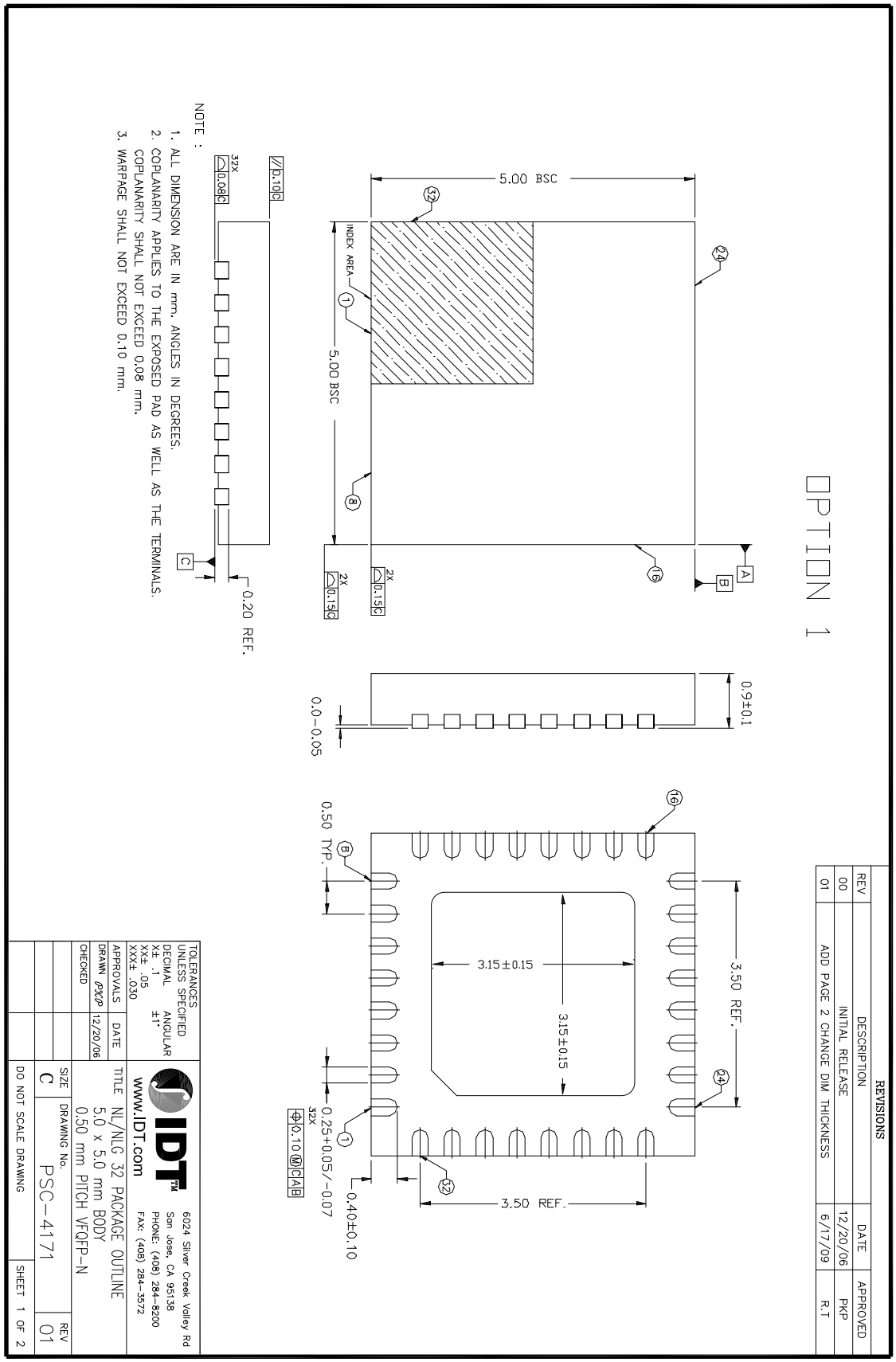
Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

Transistor Count

The transistor count for IDT8V89308I is: 22,280

32 Lead VFQFN Package Outline and Package Dimensions



Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V89308ANLGI	IDT8V89308ANLGI	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
8V89308ANLGI8	IDT8V89308ANLGI	“Lead-Free” 32 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		21	Deleted page 21, “Option 2 of NL/NLG32 package outline.” Only Option 1 is applicable to this device.	6/18/2012

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